AVID TECHNOLOGIES, INC.

June 2009 - Featured Technical Article

TECHTIP FOR FPGA DESIGN WHERE PROPER MANAGEMENT OF ASYNCHRONOUS SIGNALS IS ESSENTIAL FOR ROBUST AND RELIABLE DESIGNS

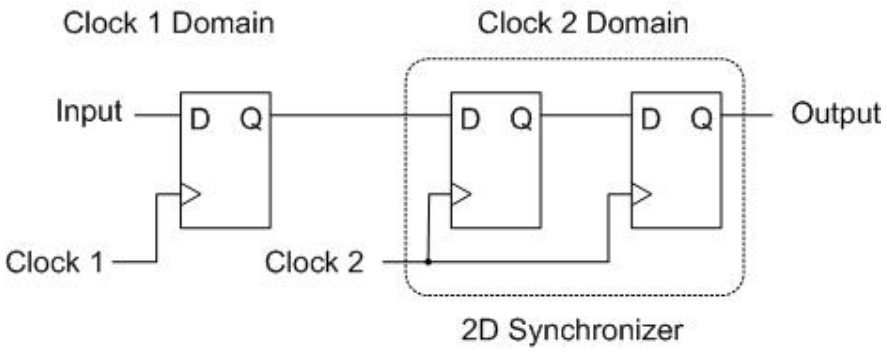
Many of the FPGA/VHDL design projects that come into AVID from our customers are efforts to convert an ASIC to FPGA, or fix or improve a prior “troubled” project. Too often we see “asynchronous” vs “synchronous” design techniques that can lead to functionality or reliability problems. Here is a basic but all-important TechTip for synchronous design.

Multiple clock domains are common in today’s FPGA designs. Moving data and control signals across clock domains can be a source of data corruption and intermittent operation. These issues can be extremely difficult to identify in system. Proper design techniques can help ensure a robust and reliable design.

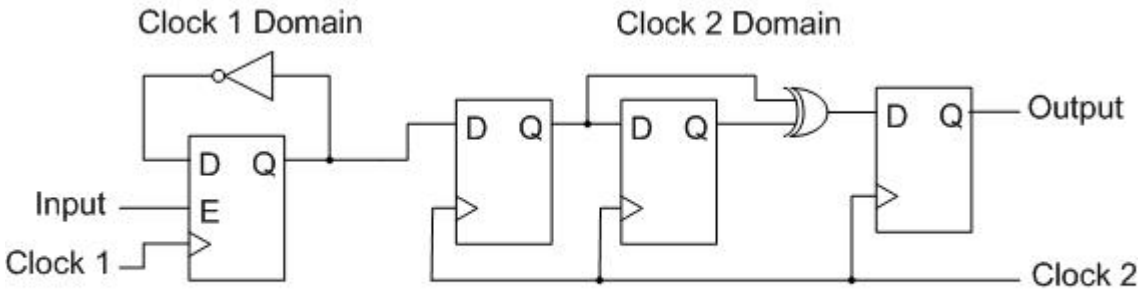
A clock domain is defined as a block of logic driven by the same clock signal. A flip-flop’s data signal must be stable for a set time, before and after the active edge of its clock. These requirements are known as a flip-flop’s setup and hold time. If these requirements are not met, the flip-flop may not transition or settle to a known state before the next clock edge occurs. This phenomenon is known as metastability. It is possible for this phenomenon to cause additional timing violations in downstream flip-flops. This extends the metastability phenomenon down data and control paths, frequently producing corruption of data and loss of control.

When data and control signals move between unrelated clock domains, the potential for metastability exists. These signals may originate from an off chip source or from a different clock domain within the design. Typically clock domains have different clock frequencies. However, regions of logic driven by clocks of the same frequency, but with an unknown phase relationship, must also be considered as different clock domains.

To minimize the failures due to metastability, a signal must be synchronized to the clock of the new clock domain. The classic solution is to use a synchronizer composed of two D flip-flops connected in series. The design ensures the first flip-flop exits its metastable state before the second flip-flop samples it. This solution is often used to bring off-chip signals into a design. To work properly, the Input signal must be stable for a duration greater than two periods of the Clock 2 Domain clock. Note that the output signal will lag the Input signal between one and two clock 2 periods. This delay is often negligible when bringing signals into a design from an off-chip source, but must be taken into consideration when moving an on-chip signal between clock domains



Often, a control signal, such as a read or write strobe, must cross clock domains. The pulse synchronizer shown below will accomplish this task. It converts a pulse in Clock Domain 1, to a pulse in Clock Domain 2. The pulse in Clock Domain 2 will be one clock tick wide. The output signal will delay the input signal by two or three clock 2 periods. The impact of this delay on system timing must be taken into consideration. Sometimes, it may be necessary to latch a corresponding data or address bus, to ensure the bus is stable when used by the circuitry of the other clock domain. Note that the pulse synchronizer can move signals from a slower to faster clock domain and vice versa. The critical requirement that must be met is that the rate of occurrence of the control signal must not occur more frequently than the duration of 3 clocks periods of the downstream clock domain.



Pulse Synchronizer

Proper management of asynchronous signals in an FPGA design can avoid a major cause of intermittent operation and lost or corrupted data, helping to ensure a robust, reliable and trouble-free development process.

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